PC Engines

apu4 series system board

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PC Engines GmbH
www.pcengines.ch

CE Declaration of Conformity

We, the undersigned,

Manufacturer: PC Engines GmbH

Address: Flughofstrasse 58, 8152 Glattbrugg, Switzerland

declare, that the product

Product name: System board apu4a4, apu4b4, apu4c2, apu4c4

conforms to the following Product Specifications and Regulations:

EMC:

EN 55032:2015/AC:2016 Class B

EN 61000-3-2:2014

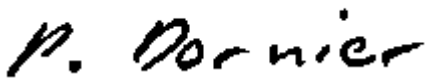
EN 61000-3-3:2013

EN 55024:2010/A1:2015

RoHS:

EN 50581:2012

The product herewith complies with the requirements of the EMC directive 2014/30/EU, and the RoHS directive 2011/65/EU and carries the CE marking accordingly.



Pascal Dornier / President

Glattbrugg, August 30, 2018

FCC Declaration of Conformity

We, the undersigned,

Manufacturer: PC Engines GmbH

Address: Flughofstrasse 58, 8152 Glattbrugg, Switzerland

declare, that the product

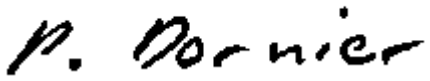
Product name: System board apu4a4, apu4b4, apu4c2, apu4c4

conforms to the following specifications:

FCC Part 15, Subpart B, Unintentional Radiators

Supplementary Information:

The device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.



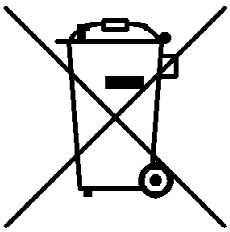
Pascal Dornier / President

Glattbrugg, August 30, 2018

Compliance notes

Test reports available on request. Please note that further compliance testing at the system level may be required for CE mark when other modules such as wireless cards are added.

Recycling / disposal



Do not discard electronic products in household trash! All waste electronics equipment should be recycled according to local regulations.

Information for the recycler:

Remove the LR44 alkaline battery for separate recycling. Our enclosures are made of aluminium.

Introduction / Features

PC Engines apu boards are small form factor system boards optimized for wireless routing and network security applications.

CPU	AMD G series GX-412TC, 1 GHz quad core (Jaguar core) with 64 bit support, AES-NI, 32K data + 32K instruction cache per core, 2MB shared L2 cache
DRAM	2 or 4 GB DDR3-1333 DRAM
Storage	Boot from SD card (built-in adapter, connected through USB), USB or m-SATA SSD. 1 SATA data + power connector.
Power	12V DC, 2.5 mm center pin, center positive. About 6 to 10W depending on CPU load. Recommend 12V adapter rated for at least 1.5A to provide margin for peripherals.
Expansion	3 miniPCI express (two with SIM socket for 3G modem), LPC bus, GPIO header, optional I2C bus, COM2 (3.3V RXD/TXD).
Connectivity	4 Gigabit Ethernet (Intel i211AT), 1 DB9 serial port (console).
Firmware	CoreBoot open source system BIOS with support for iPXE and USB boot.
Form factor	6"x6" (152.4 x 152.4 mm), fits in our case1d2*u enclosures.
Cooling	Conductive cooling from the CPU to the enclosure.

Heat spreader assembly

The apu CPU is passively cooled by heat conduction to the enclosure. This requires correct installation of a heat spreader.

The board should not be operated without CPU cooling except for brief bench tests.

The included heat spreaders are designed for our enclosures. Third party enclosures should work if they are made from aluminium, and have a board standoff height of 5 mm. If in doubt, please contact us. Based on our measurements, at full load the CPU runs a few degrees cooler in the black (case1d2blku) or red (case1d2redu) enclosures, compared to the plain anodized enclosure (case1d2u).

Photos for this assembly procedure can be found at www.pcengines.ch/apucool.htm .

- Remove DB9 hex nuts using a suitable tool (such as our hexbit tool, or a simple plier).
- Using a small x-acto knife or tweezer, peel transparent backing foil from the small blue heat conductive pad. Apply to the CPU. Then peel the blue cover foil from the heat conductive pad.
- Place the alu heat spreader (blank side down) over the CPU. Make sure to avoid conflict with nearby through hole components. Peel the cover foil.

  Or

  Use our apufix heat spreader placement template to position the heat spreader, and stick it in the enclosure.
- "Bottoms up" - hold the enclosure base upside down, feed the board DB9 and LAN connectors through the openings. Lightly press board and enclosure base together to stick the heat spreader in place.
- Turn around and carefully press down around CPU and heat sink to get good contact between enclosure and heat spreader. Then insert screws and hex nuts.

Please do not disassemble the unit needlessly, the thermal conductive pads are easily damaged. Replacement blue pads (free) or complete heat spreader kits (nominal charge + shipping cost) are available from us on request.

Getting started…

- Please install heat spreader as described in the prior section.
- Insert a boot device (SD card, mSATA SSD, USB stick, or PXE through LAN).
- Connect serial port to a PC through null modem cable (RXD / TXD crossed over). Set terminal emulator to 115200 8N1.
- Connect Ethernet as needed.
- Connect a 12V DC power supply to the DC jack. Power supply should be able to supply at least 18W (1.5A) for some margin. To avoid arcing, please plug in the DC jack first, then plug the adapter into mains.

The board should now power on. All three LEDs will light during BIOS POST, then the system will try to boot. You should see BIOS messages on the serial console. Press F10 for boot device selection. For example:

```
   PC Engines apu4
   coreboot build 20171130
   BIOS version v4.6.4
   4080 MB ECC DRAM

   SeaBIOS (version rel-1.11.0.1-0-g90da88d)

   Press F10 key now for boot menu:

~~~

   Select boot device:
   1. SD card SD04G 3796MiB
   2. Payload [memtest]
   3. Payload [setup]
```

Setup options

To set up the boot sequence and other options, press F10 for boot device selection, then select Payload [setup].

```
   Boot order - type letter to move device to top.

     a USB 1 / USB 2 SS and HS
     b SDCARD
     c mSATA
     d SATA
     e mPCIe1 SATA1 and SATA2
     f iPXE (disabled)


     r Restore boot order defaults
     n Network/PXE boot - Currently Disabled
     u USB boot - Currently Enabled
     t Serial console - Currently Enabled
     o UART C - Currently Enabled
     p UART D - Currently Enabled
     m Force mPCIe2 slot CLK (GPP3 PCIe) - Currently Disabled
     h EHCI0 controller - Currently Disabled
     w Enable BIOS write protect - Currently Disabled
     x Exit setup without save
     s Save configuration and exit
```

The lower case letters will change the boot sequence, pull the selected device to the top of the list.

Caution: Serial console disable does not work correctly on the current BIOS. BIOS update will be required to use this feature.

Memtest

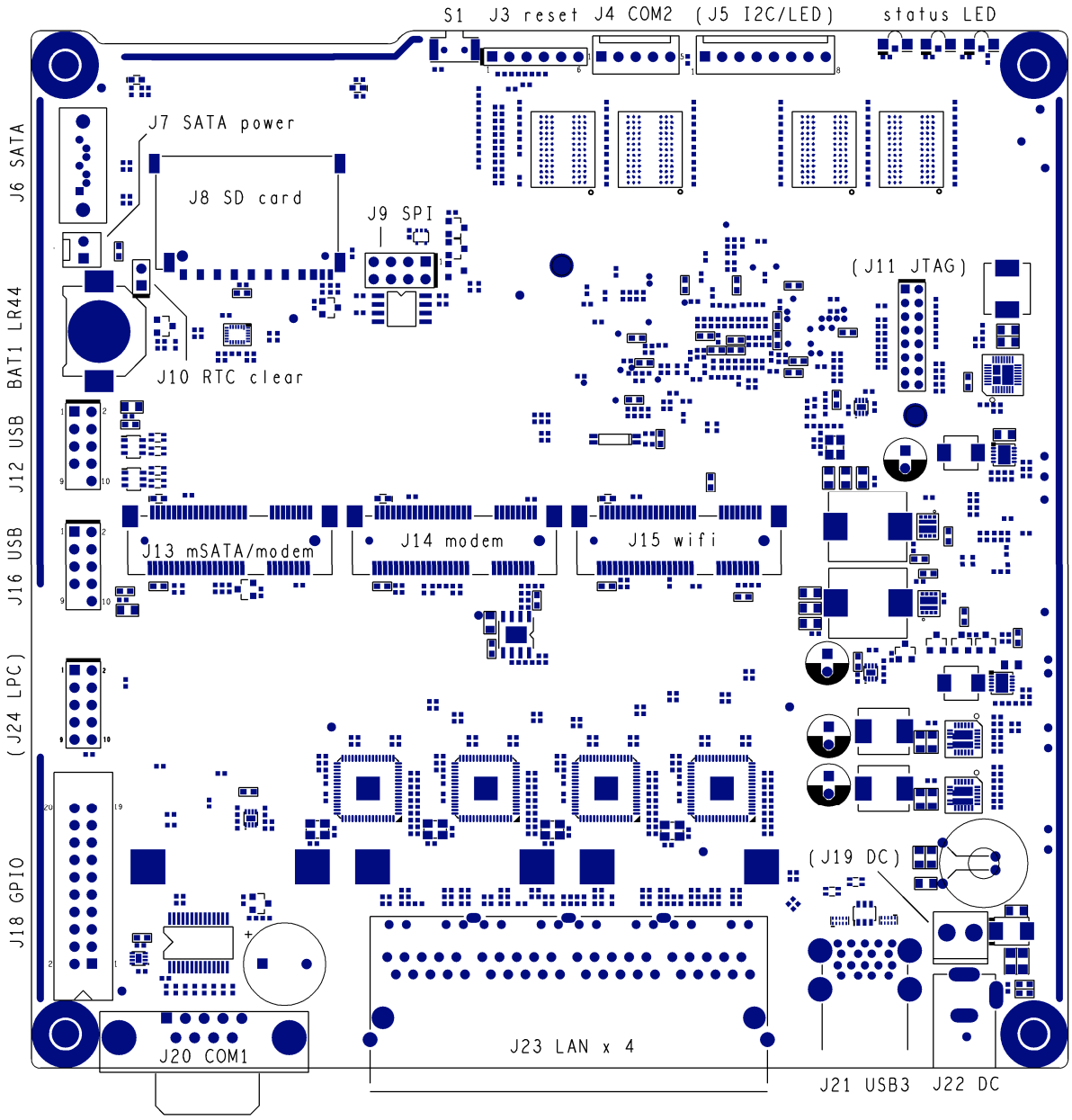
To start, press F10 for boot device selection, then select Payload [memtest].

BIOS update

Please see www.pcengines.ch/howto.htm .

For “debricking”, place our spi1a module on header J9, boot from SD card or USB, and reprogram the BIOS.

Connectors



BAT1 battery	LR44 1.5V alkaline battery for RTC / CMOS
J1 SIM	(bottom side) – SIM socket for 3G modem installed in miniPCIe J14. Can be swapped with J2 SIM under software control (no SIM switch on apu4c2).
J2 SIM	(bottom side) – SIM socket for 3G modem installed in miniPCIe J13. Can be swapped with J1 SIM under software control (not installed on apu4c2).
J3 power / reset	Pins 1-2 = reserved Pins 2-3 = power button Pins 4-5 = reset button

	Pins 5-6 = reserved
J4 COM2	3.3V serial port (RXD / TXD only).
(J5 I2C / LED)	(optional expansion, see schematic for pinout)
J6 SATA	For SATA devices.
J7 SATA power	5V power for SATA devices.
J8 SD card	SD card interface, driven by AMD SOC, use sdhci driver.
J9 SPI	SPI header for debricking. Do not connect pins 7 / 8 for Dediprog use.
J10 CMOS reset	Short these pins while power is off to clear RTC / CMOS RAM. Don't leave jumper permanently as this would drain the battery.
(J11 JTAG)	Debug only, not populated.
J12 USB	Internal USB (2 x USB 2.0) – present on apu4c and later.
J13 mSATA / miniPCI express	This slot can be used for mSATA SSD, or 3G/LTE modem (USB based). No PCI express = no wifi. Connects to SIM J2.
J14 miniPCI express	This slot can be used for 3G/LTE modems (USB based). No PCI express = no wifi. Connects to SIM J1.
J15 miniPCI express	This slot includes PCI express, and is intended for wifi modules. No SIM connected.
J16 USB	Internal USB (2 x USB 2.0)
J18 GPIO	General purpose I/O pins + extra serial ports, driven by Nuvoton NCT5104D I/O controller. Data sheet and sample code available on request.
(J19 internal power)	Optional power header, designed for 0.156" pitch header (Digi-Key part A1971-ND).
J20 COM1	Serial port with full handshake signals.
J21 USB	External USB (2 x USB 3.0)
J22 Power	DC jack (2.5 mm center pin, center positive).
J23 LAN1..4	GigE port. Left LED (green) indicates activity, right LED (amber) is turned on when the connection is Gigabit.
J24 LPC	Minimal LPC header for debug and TPM (apu4c and later).

Hardware notes

For detailed pinouts, full board schematics are available on our web site.

Hardware limitations

This board does not support power over Ethernet.

GPIO

The following signals are driven by the AMD FCH south bridge function:

Pushbutton switch S1 = G32

LED1 = G57, LED 2 = G58, LED 3 = G59

SIM switch (not present on apu4c2) is controlled by G33, 0 = swap, 1 = normal connection.

GPIO pins on header J20 are driven by the Nuvoton NCT5104D I/O controller. Data sheet and sample code available on request.

CoreBoot source code

The CoreBoot firmware is licensed under the GPL. To obtain the source code and a Voyage Linux image with the tool chain needed to compile it, please contact support@pcengines.ch .